WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first layer;

a plurality of first test elements which are arranged in the first layer;

a second layer which is adhered to the first layer and is different from the first layer; and

a plurality of pads which are arranged in the second layer and electrically connected to the first test elements.

2. The device according to claim 1, further comprising:

a plurality of bumps which are respectively arranged on the pads;

a third layer which is adhered to the second layer via the bumps and is different from the first and second layers; and

solder balls which are arranged on the third layer and electrically connected to the first test elements.

3. The device according to claim 1, wherein all the first test elements are of the same type.

4. The device according to claim 1, wherein the first test elements are arranged in a first line.

5. The device according to claim 1, further comprising a plurality of second test elements which are arranged in the first layer and electrically insulated from the pads.

6. The device according to claim 5, wherein all the second test elements are of the same type.

7. The device according to claim 5, wherein the second test elements are of a type different from the first test elements.

8. The device according to claim 5, wherein the first test elements are arranged in a first line, and the second test elements are arranged in a second line different from the first line.

9. The device according to claim 5, wherein the second test elements are arranged in the first layer below the pads.

10. The device according to claim 1, further comprising:

a first connection member which is arranged in the first layer and connected to the first test elements; and

a second connection member which is arranged in the second layer and connected to the pads and the first connection member.

11. The device according to claim 2, further comprising:

a first connection member which is arranged in the first layer and connected to the first test elements;

a second connection member which is arranged in the second layer and connected to the pads and the first connection member; and

a third connection member which is arranged in the third layer and connected to the bumps and the solder balls.

12. A semiconductor device manufacturing method comprising:

forming a first layer and a second layer being different from the first layer, the first layer having a plurality of first test elements, the second layer having a plurality of pads; and

adhering the first and second layers to electrically connect the first test elements to the pads.

13. The method according to claim 12, further comprising:

respectively forming a plurality of bumps on the pads in forming the second layer;

forming a third layer having solder balls separately from formation of the first and second layers; and

after adhering the first and second layers, adhering the second and third layers to electrically connect the first test elements to the solder balls via the bumps.

14. The method according to claim 12, wherein all the first test elements are of the same type.

15. The method according to claim 12, wherein the first test elements are formed in a first line.

16. The method according to claim 12, wherein in forming the first layer, a plurality of second test elements which are electrically insulated from the pads are formed in the first layer.

17. The method according to claim 16, wherein all the second test elements are of the same type.

18. The method according to claim 16, wherein the second test elements are of a type different from the first test elements.

19. The method according to claim 16, wherein the first test elements are formed in a first line, and the second test elements are formed in a second line different from the first line.

20. The method according to claim 16, wherein the second test elements are formed in the first layer below the pads.

21. The method according to claim 12, further comprising:

forming in the first layer a first connection member which is connected to the first test elements in forming the first layer; and

forming in the second layer a second connection member which is connected to the pads and the first connection member in forming the second layer.

22. The method according to claim 13, further comprising:

forming in the first layer a first connection

member which is connected to the first test elements in forming the first layer;

forming in the second layer a second connection member which is connected to the pads and the first connection member in forming the second layer; and

forming in the third layer a third connection member which is connected to the bumps and the solder balls in forming the third layer.

23. A semiconductor device test method comprising:

forming a first layer and a second layer being different from the first layer, the first layer having a plurality of first test elements, the second layer having a plurality of pads;

adhering the first and second layers to electrically connect at least some of the test elements to the pads; and

evaluating performance of said at least some of the test elements.

24. The method according to claim 23, further comprising:

respectively forming a plurality of bumps on the pads in forming the second layer;

forming a third layer having solder balls separately from formation of the first and second layers; and

after adhering the first and second layers, adhering the second and third layers to electrically

connect said at least some of the test elements to the solder balls via the bumps.

25. The method according to claim 23, wherein test elements of the same type are formed in a line.

26. The method according to claim 25, wherein test elements of the same type are evaluated.